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(54) High frequency semiconductor device.

(57) A high frequency semiconductor device comprising metal electrode leads (32) formed on one surface of a flexible film (30), a plurality of bumps (34) partially formed on the electrode patterns, a recessed portion (35) formed on the flexible film among the plurality of bumps and a plurality of electrode pads of the high frequency semiconductor device bonded to the bumps in correspondence to each other.

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HIGH FREQUENCY SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a high frequency semiconductor device, and more particularly to packaging which can provide the semiconductor device with an excellent high frequency characteristic.

Referring to figs. 6A and 6B, the previously method for packaging a transistor for a high frequency of 3 GHz or higher, particularly a GaAs-FET (field effect transistor) will be explained. As shown in Figs. 6A and 6B, a GaAs-FET chip 100 is sealed within a package consisting of a base 101 and a cap 107 both of which are made of alumina ceramic. In Figs. 6A and 6B, 102 are bonding wires, and 103A, 103B and 103C are Au-plated layers with which a drain electrode lead 104, a source electrode lead 15 and a gate electrode lead 106 are connected, respectively.

The schematic process for packaging such a GaAs-FET is shown in Fig. 7 of the flow chart. In Step 1, the back surface of a GaAs wafer, which has been ground and shaped to a prescribed thickness, is metallized with e.g. Au on which solder for dice bonding is to be applied. In Step 2, the wafer is scribed and broken into a number of chips. In Step 3, each of the chips is dice-bonded on the Au-plated layer 103B using the solder such as Au/Sn solder. In Step 4, wire-bonding is made for each of the chips by using bonding wires 102. In this step, to make the source inductance as small as possible is important for improving the high frequency characteristic, particularly, the noise factor (F) and the gain (Ga). For this purpose, the length of bonding wires 102s is made as short as possible, and the number of the wire bondings is increased (4 in fig. 6A). Finally, in Step 4, the cap 107 is bonded to the base 101.

Meanwhile, the reduction in cost for fabricating microwave semiconductor packages have been eagerly demanded; this demand is so great that it cannot be satisfied only by reducing the cost for semiconductor ships themselves. So the reduction in cost required for assembling the semiconductor chip or packaging it has been eagerly demanded. Some microwave packages occupy in their assembling and mounting cost almost half the entire cost of the semiconductor device. However, the reduction in cost is limited as long as the conventional ceramic package is used. Further, the high performance of the semiconductor devices has been further required; this requirement cannot be also satisfied by only improving the chips themselves, and so must be satisfied in the viewpoint of packaging. For example, in order to shorten the length of the above source wire, the "flip-chip bonding" technique has been proposed for a power FET; in the flip-chip bonding technique, bumps formed on the electrodes of a ceramic package are bonded with the pads on a chip which are provided in opposition to the bumps. However, this technique, which improves the performance but uses the ceramic package, is still expensive since it requires a step of forming bumps on the expensive ceramic body and cannot satisfy the requirement of low cost.

In view of such inconvenience, an object of the present invention is to provide a package which can realize the high frequency characteristic of a semiconductor device by low cost.

In order to attain this object, in accordance with the present invention, there is provided a high frequency semiconductor device comprising metal electrode patterns formed on one surface of a flexible film, a plurality of bumps partially formed on the electrode pattern, and a plurality of electrode pads of the high frequency semiconductor device bonded to the bumps in opposition to each other. In this case, a recessed portion is formed on the flexible film among the plurality of bumps. Preferably, the surface of a recessed portion formed on the flexible film is partially covered with the metal electrode pattern to be connected with the electrode pads.

Further, in accordance with the present invention, there is provided a high frequency semiconductor device comprising a plurality of lead frames, a plurality of bumps partially formed on a surface of lead frames one of which has a recessed portion among the bumps. Moreover, a plurality of electrode pads of the high frequency semiconductor device are bonded to the bumps in correspondence to each other.

In accordance with the present invention, the above flip-chip bonding technique, in which a high frequency semiconductor chip is bonded onto a metal pattern in the state laid facedown which is opposite to the ordinary manner, can be carried out on a film carrier.

Further, use of metallic bumps permits not only the ordinary wire bonding step to be omitted but also the source inductance, which deteriorates the high frequency characteristic of the semiconductor device, to be restrained. Furthermore, use of the film carrier and provision of the bumps thereon permits the semiconductor device to be completed with very lower cost than the ceramic package, and also the floating capacitance to be restrained as compared with use of the ceramic carrier; this is very advantageous to realize the high performance of the semiconductor device.

Further, in accordance with the present invention, air isolation using a recessed portion (gap) is made

for electrical isolation between the input and output of the semiconductor device, which is particularly essential for the high frequency semiconductor device, so that the electrical isolation performance can be greatly improved. Further, in accordance with the present invention, bumps are formed on a film carrier lead or a lead frame and thereafter the semiconductor chip is sealed to provide leads, so that the package can be provided at low cost.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a plan view of the main part of a semiconductor device according to one embodiment of the present invention;

Fig. 1B is a sectional view taken along line A - A′ of Fig. 1A;

Fig. 2 is an enlarged perspective view in the neighborhood of the bumps of the semiconductor device of Figs. 1A and 1B;

Fig. 3A is a plan view of the main part of a modified semiconductor device in which the semiconductor chip is molded by resin in place of being sealed by the ceramic case shown in Figs. 1A, 1B and 2.

Fig. 3B is a sectional view taken along line B - B′ of Fig. 3A.

Fig. 4A is a plan view of the main part of a semiconductor device according to another embodiment of the present invention;

Fig. 4B is a sectional view taken along line C - C′ of Fig. 3A;

Fig. 5 is an enlarged perspective view of the semiconductor device of Fig. 4A;

Figs. 6A and 6B are a plan view and a sectional view of the prior art semiconductor device; and

Fig. 7 is a flowchart of the prior art process of assembling a semiconductor device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now referring to the drawings, several embodiments of the present invention will be explained.

Embodiment 1

As shown in Figs. 1A and 1B, electrode leads 32 of metal patterns are formed on one main surface of a flexible film 30 of polyimide, bumps 34 of gold are formed on the required positions on the electrode leads 32 by the technique such as duplicating bumping. For example, in this embodiment, the bumps 34 are formed on the leads 32 in alignment with the bonding pads of a GaAs-FET 31 chip as a high frequency semiconductor device for processing a signal at 3 GHz or higher. In the duplicating bumping, the bumps 34 can be formed by first forming bumps on a glass plate (not shown), bonding the bumps on the metal leads 32 and detaching the glass place from the bumps so that the bumps are duplicated onto the metal leads 32. The bumps 34 may be also formed on the leads 32 by the technique other than the duplicating bumping. The GaAs-FET, which is a semiconductor chip, is positioned under recognition of the bumps 34 of the electrode leads 32 and the electrode pads on FET 31 for single bonding thereto. Additionally, 35 is a gap or recessed portion formed on the flexible film 30 between the bumps 34. A cap 36 of ceramic as shown in Fig. 1B is not shown in Fig. 1A. In the leads 32 shown in Fig. 1A, S is a source lead; D is a drain (output) lead; and C is a gate (input) lead.

Fig. 2 is an enlarged perspective view in the neighborhood of the bumps 34. In this embodiment, the height and diameter of the gold bumps 34 are set for 50 to 100 μm and 500 μmø, respectively. The height of the bumps 34 must be set for a value larger than a prescribed value; if not, the parasitic capacitance is increased to deteriorate the characteristic of the semiconductor device.

In this embodiment, it is not necessary to form bumps on the expensive high frequency semiconductor device, and the polyimide film as a flexible film, which is less expensive and has a lower permitivity than alumina ceramic used in the ordinary ceramic package, is used so that the semiconductor device can be realized with a low floating capacitance at very low cost.

Meanwhile, in order for the semiconductor device to acquire excellent high frequency performance, it is essential to be able to take electrical isolation, which is represented by $-|S_{12}|$, between the input and output of the semiconductor device. The degree of isolation substantially depends on the coupling capacitance between the input and output. Where the input/output electrodes are formed on the polyimide film as in this embodiment, the isolation will be deteriorated because of the absence of an earth pattern for shielding

between the input and output unlike the prior art as shown in Figs. 6A and 6B. In the FET 31 chip actually used, its source and drain are very near to each other (the distance therebetween is very short as about 3 μm) so that the degree of the isolation at this portion is critical for the high frequency semiconductor device. In this embodiment, in order to obviate this, as shown in Fig. 1B, a recessed portion (gap) 35 having a depth of about 200 μm - 300 μm is formed between the input electrode and output electrode on the flexible film 30; without the presence of e.g. resin having large permittivity the input and output are isolated by an air layer thus formed to enhance the degree of isolation. Further, the source electrode lead 32 (S) is extended on the surface of the gap 35 to provide the shielding effect so that the degree of electric isolation can be further enhanced. Thus, in an example of packaging a HEMT semiconductor chip which is a kind of GaAs FET the degree of isolation can be improved by 5 dB in a Ku band as shown in the following table. This result is very advantageous for the high frequency semiconductor device for 9GHz or higher. Also, the noise factor NF can be improved by 0.1 dB.

Table

	ISOLATION	NF
THIS EMBODIMENT (PRESENCE OF GAP)	-25 dB	0.8 dB
NO GAP	-20 dB	0.9 dB
(measured at the frequency of 12 GHz)		

The semiconductor chip 3 bonded to the electrode leads 32 on the flexible film 30 through the bumps 34 is sealed by the ceramic cap 36. Such sealing is incomplete to remove humidity; however, this is not significant as long as the semicondcutor chip 31 is completely passivated by SiN. The package constructed in accordance with this embodiment is not so different from the conventional ceramic package in appearance so that the completed semiconductor device can be mounted in a circuit in substantially the same way as the conventional process.

Further, the semicondcutor chip may be molded by resin as shown in Figs. 3A and 3B or covered with a flexible resin film in place of being sealed by the ceramic case 60.

Embodiment 2

Figs. 4A and 4B shows the high frequency semiconductor device according to still another embodiment of the present invention; this embodiment provides a beam lead type semiconductor device. Fig. 5 shows an enlarged view of the semiconductor device in the neighborhood of the bumps 34. As seen from Fig. 5, bumps 34 are formed on leads 62 to be constructed by a lead frame by e.g. the duplicating bumping technique as mentioned previously. The respective leads are made integral at the position not shown.

The process for fabricating the semiconductor device according to this embodiment will be explained. First, as seen from Fig. 4B, in order to provide the shielding effect between the input and the output of the FET chip 31, or between the gate and drain thereof, the source electrode lead 62 (S) is bent to provide a recessed portion or gap 35. Thereafter, bumps are attached on the leads as shown in Figs. 4A and 5. The source electrode lead 62 (S) is not required to be bent to provide a recessed portion as long as the bumps 34 are 50 μm or higher. Next, as seen from Figs. 4A and 4B, a ceramic case 60 is attached to sandwich the leads 32. Finally, the integral portion (not shown) of the leads, i.e. a part of the lead frame is cut to separate the leads individually. In this way, the beam lead type semiconductor device is completed. The semiconductor chip, in place of being sealed by the ceramic case 60, may be molded by resin as shown in Figs. 3A and 3B or covered with a flexible resin film. The beam lead type semiconductor device thus completed has advantages of very small size and low cost (about half the conventional device using the ceramic package).

In accordance with the present invention, a very excellent high frequency characteristic and low cost can be realized simultaneously for the high frequency semiconductor device for 3 GHz or higher. This is advantageous for reducing the production cost of an SHF converter used in broadcasting-by-satellite or satellite communication. Thus, the present invention has high industrial value in fabricating the high frequency semiconductor device with high performance.

Claims

1. A high frequency semiconductor device comprising metal electrode patterns (32) formed on one surface of a flexible film (30), a plurality of bumps (34) partially formed on the electrode patterns, a recessed portion (35) formed on the flexible film among the plurality of bumps and a plurality of electrode pads of the high frequency semiconductor device bonded to the bumps in opposition to each other.

2. A high frequency semiconductor device according to claim 1, wherein the surface of a recessed portion formed on the flexible film is partially covered with the metal electrode pattern to be connected with the electrode pads and said pattern is provided between an input and an output to constitute a shield electrode therebetween.

3. A high frequency semiconductor device according to claim 1 or 2, wherein said semiconductor device is covered with a ceramic case to be hollow-sealed.

4. A high frequency semiconductor device comprising:
a plurality of lead frames (62), a plurality of bumps (34) partially formed on a surface of each of said lead frames, one of said lead frames having a recessed portion (35) among the said plurality of bumps and a plurality of electrode pads of the high frequency semiconductor device being bonded to said bumps in correspondence to each other.

5. A high frequency semicondcutor device according to claim 4, wherein said semiconductor device is covered with a ceramic case to be hollow-sealed.

FIG. 1A

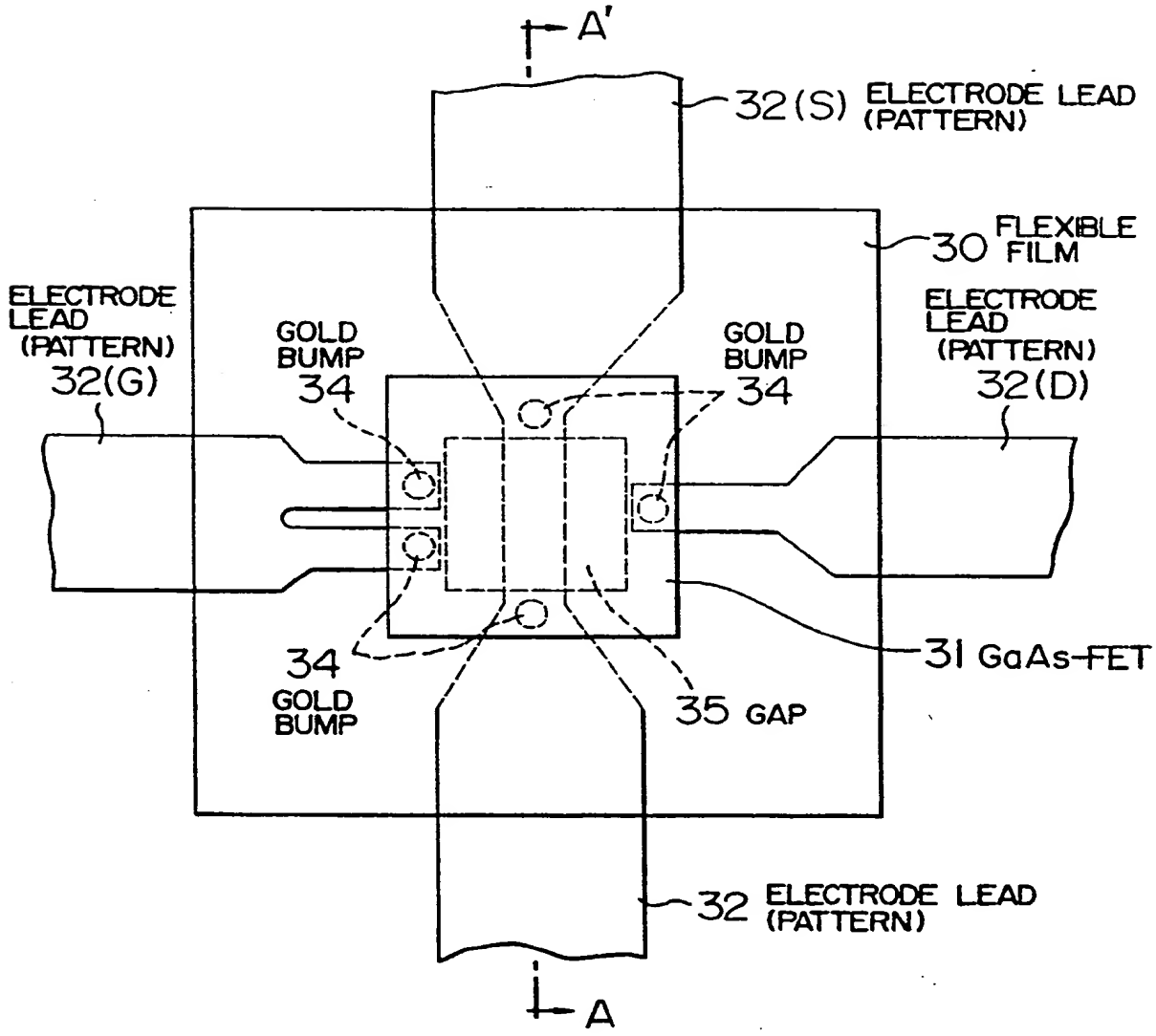

FIG. 1B

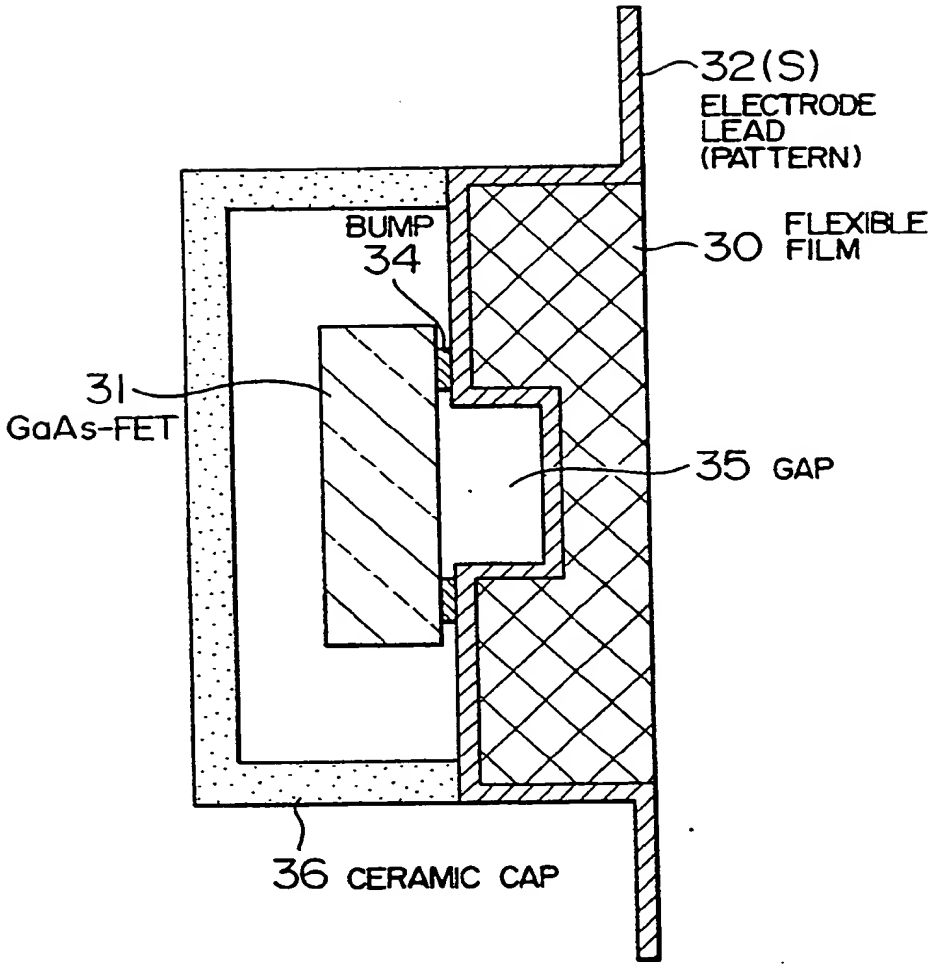
32(S)
ELECTRODE
LEAD
(PATTERN)
BUMP
34
30 FLEXIBLE
FILM
31
GaAs-FET
35 GAP
36 CERAMIC CAP

FIG. 2

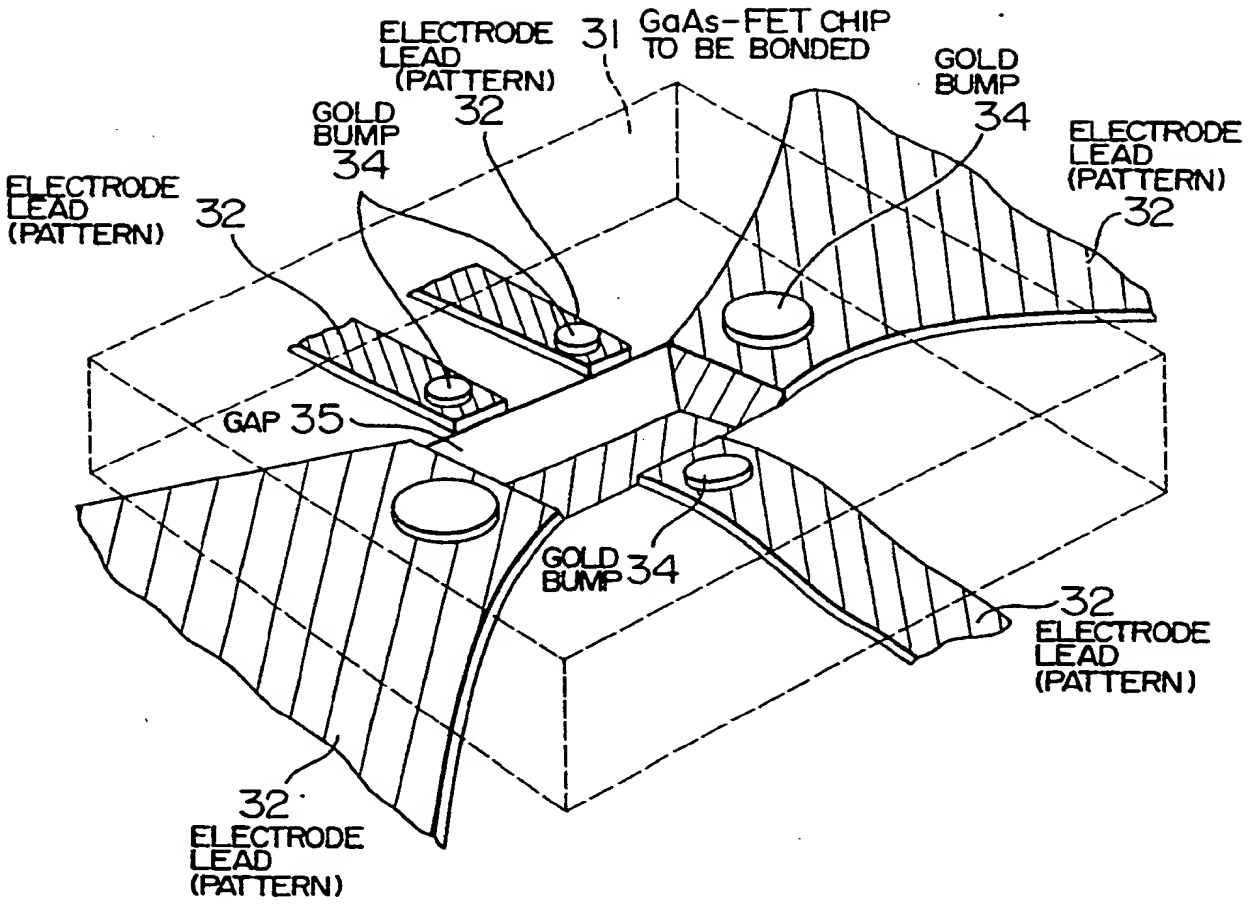

FIG. 3A

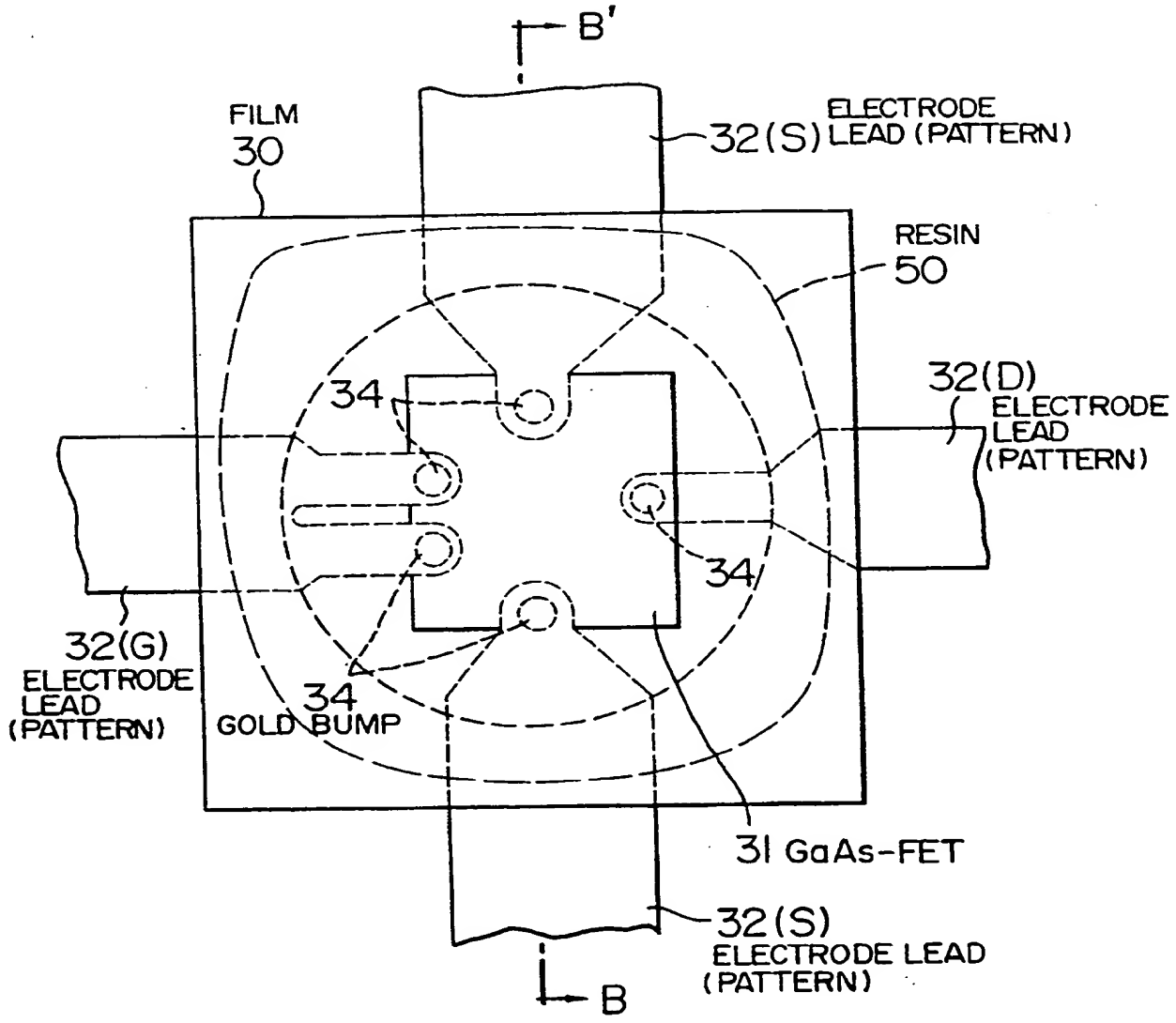
B'
FILM
30
32(S) ELECTRODE LEAD (PATTERN)
RESIN
50
34
32(D)
ELECTRODE
LEAD
(PATTERN)
34
32(G)
ELECTRODE
LEAD
(PATTERN)
34
GOLD BUMP
31 GaAs-FET
32(S)
ELECTRODE LEAD
(PATTERN)
B

FIG. 3B

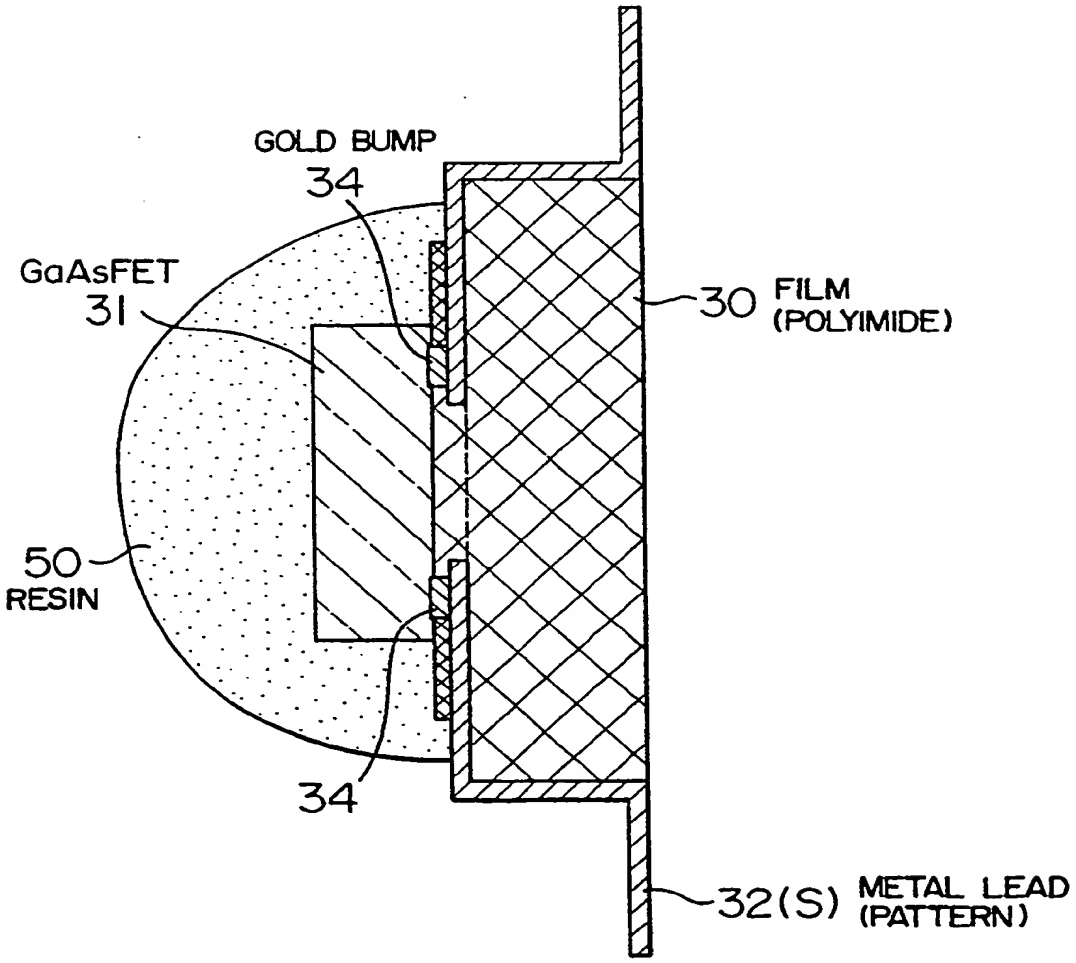

FIG. 4A

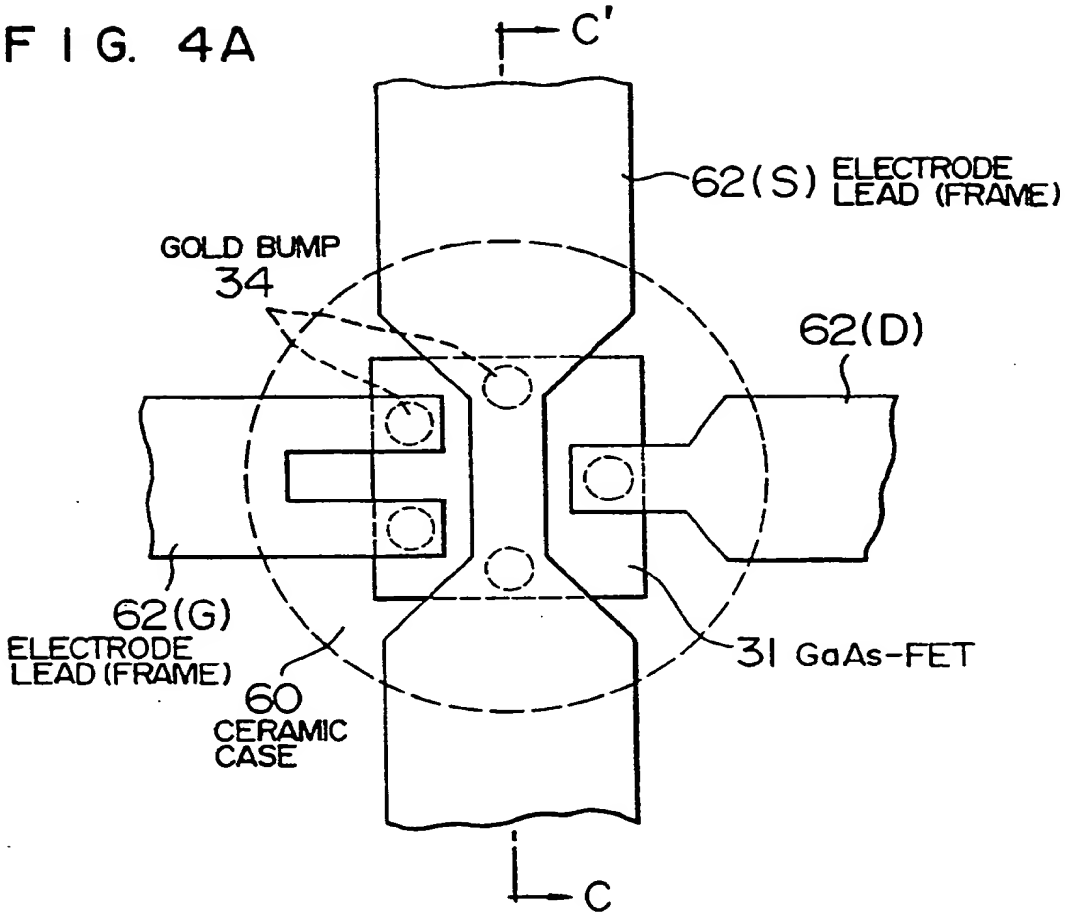
C'
62(S) ELECTRODE LEAD (FRAME)
GOLD BUMP 34
62(D)
62(G) ELECTRODE LEAD (FRAME)
60 CERAMIC CASE
31 GaAs-FET
C

FIG. 4B

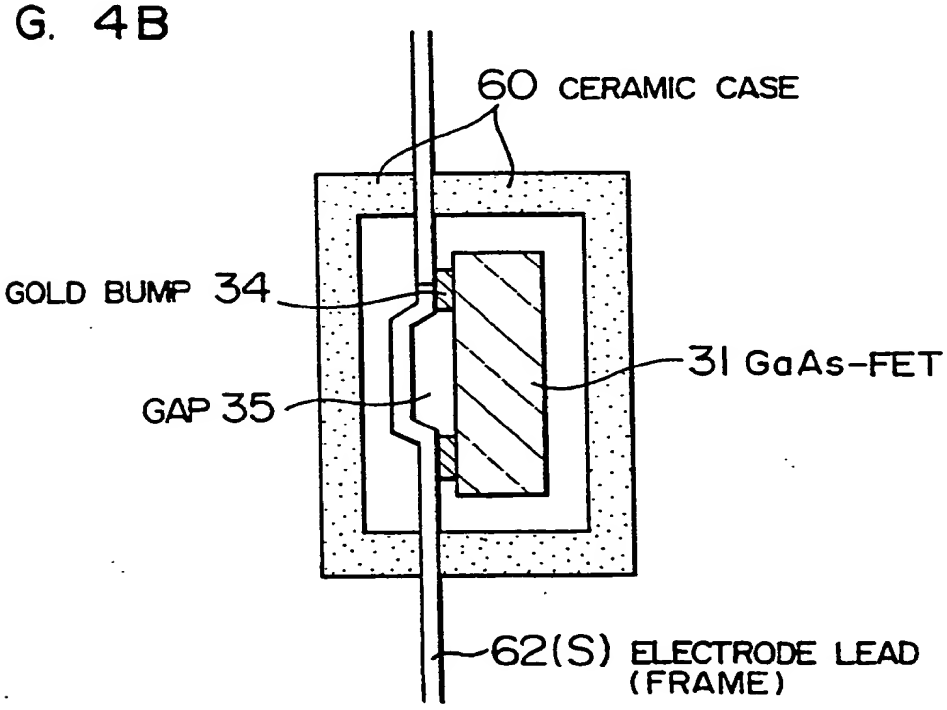
60 CERAMIC CASE
GOLD BUMP 34
31 GaAs-FET
GAP 35
62(S) ELECTRODE LEAD (FRAME)

FIG. 5

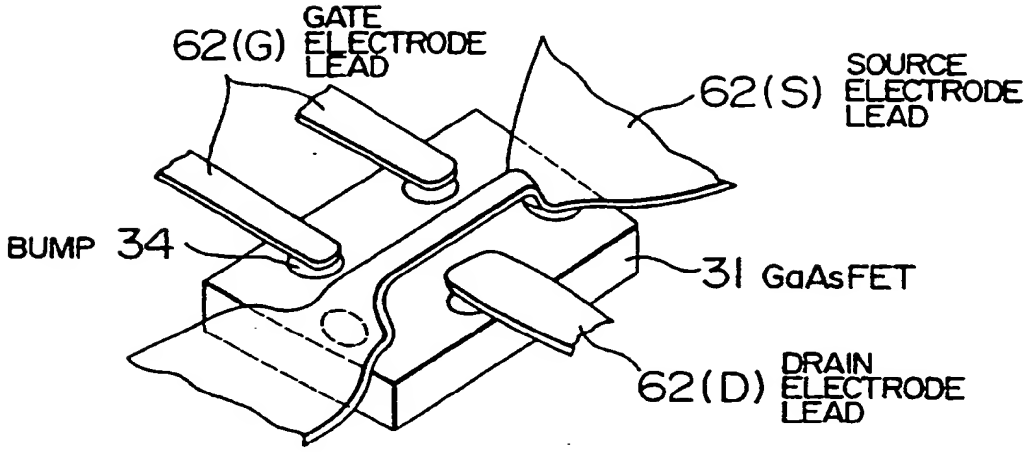

FIG. 6A
(PRIOR ART)

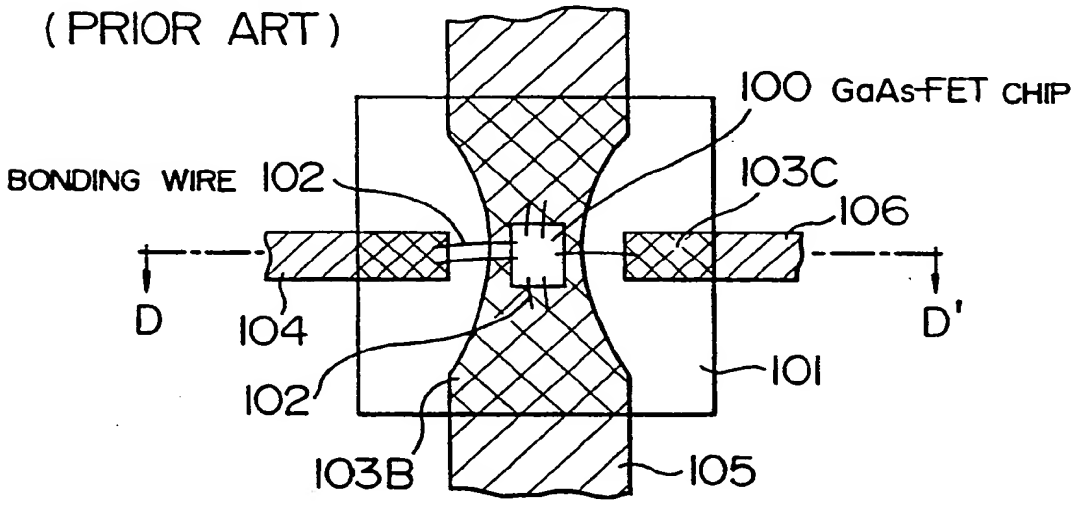

FIG. 6B
(PRIOR ART)

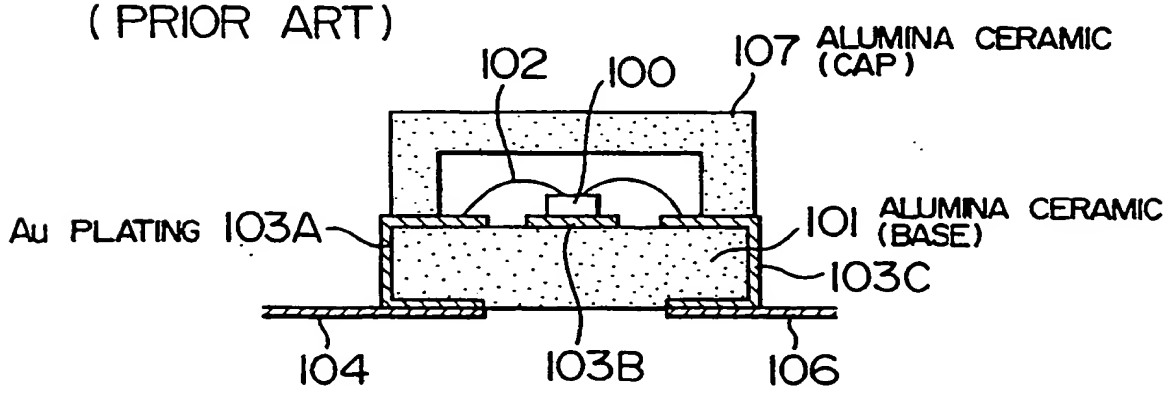

FIG. 7
(PRIOR ART)

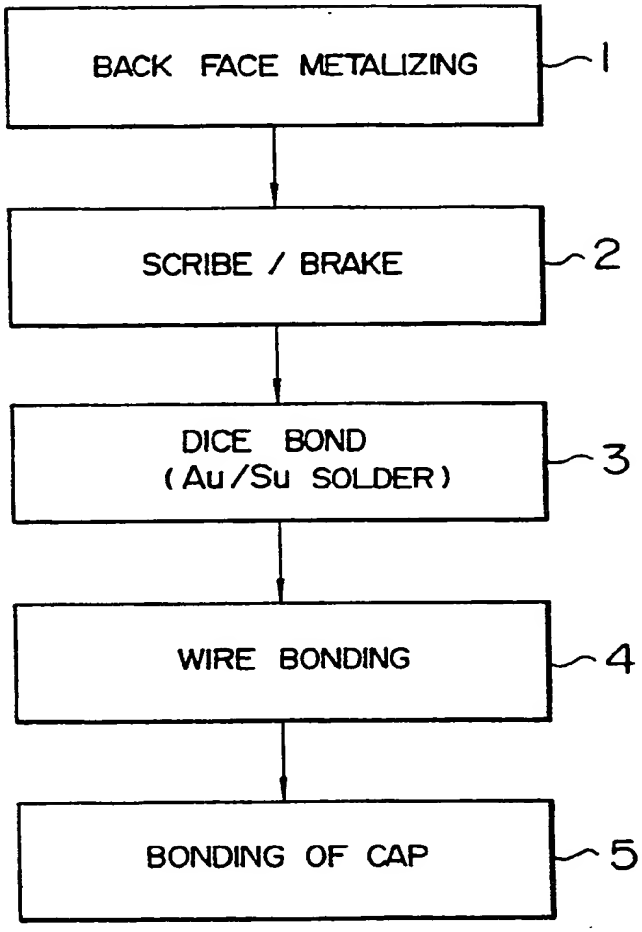

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FIG. 1A

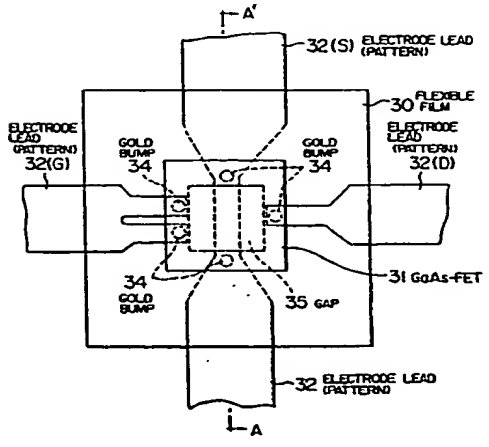
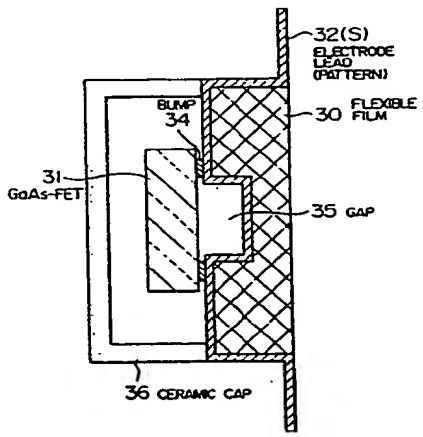


FIG. 1B



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European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 90 10 7258

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	US-A-4 612 566 (ALPS ELECTRIC CO.) * column 2, line 55 - column 3, line 4; figure 4 *	1	H 01 L 23/66 H 01 L 23/057
A	PATENT ABSTRACTS OF JAPAN vol. 13, no. 312 (E-788) 17 July 1989, & JP-A-10 84624 (TOSHIBA CORP.) 29 March 1989, * the whole document *	1	
A	PATENT ABSTRACTS OF JAPAN vol. 10, no. 329 (E-452) 08 November 1986, & JP-A-61 135211 (MITSUBISHI ELECTRIC CORP.) 23 June 1986, * the whole document *	1	
A	SIEMENS COMPONENTS. vol. XXIII, no. 2, April 1988, MUNCHEN DE pages 64 - 67; J. HAMMERSCHMITT: "MICROWAVE SEMICONDUCTORS FOR SMT" * figure 1 *	1	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 01 L

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	05 March 91	ZEISLER P.W.

CATEGORY OF CITED DOCUMENTS

X: particularly relevant if taken alone
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E: earlier patent document, but published on, or after the filing date
D: document cited in the application
L: document cited for other reasons

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